AMENDMENTS TO THE CLAIMS

Claims 1 - 53. (Cancelled)

Claim 54. (Previously Presented)

A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector

layering a top injector adjacent to the bottom injector, such that the top injector is

separated by an offset from the bottom injector; and

layering a material between the bottom injector and top injector which serves as a tunnel

barrier, wherein the bottom injector layer, the top injector layer, and said material form a p-i-n

junction, where i represents at least one material provided between the bottom injector and the

top injector.

Claim 55. (Previously Presented)

A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector;

layering a bottom spacer;

layering a top spacer;

layering a top injector adjacent to the bottom injector, the bottom injector and top injector

layers forming a p-i-n junction; and

layering a material between the bottom injector and top spacers which serves as a tunnel

barrier, wherein the bottom injector layer, the top injector layer, and said material form a p-i-n

2 MKM/CJB/cb

Reply to Office Action of September 6, 2005

junction, where i represents at least one material provided between the bottom injector and the

top injector.

Claim 56. (Withdrawn)

A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector;

layering a bottom spacer;

layering a top spacer;

layering a top injector adjacent to the bottom injector, the bottom injector and top injector

layers forming a p n junction; and

layering a material between the bottom injector and top injector which serves as a tunnel

barrier; and

wherein a quantum well is formed adjacent to the bottom injector layer and the tunnel

barrier.

Claim 57. (Withdrawn)

A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector;

layering a bottom spacer;

layering a top spacer;

layering a top injector adjacent to the bottom injector, the bottom injector and top injector

layers forming a p n junction; and

3 MKM/CJB/cb

Docket No.: 3531-0103P

layering a material between the bottom injector and the top

injector which serves as a tunnel barrier;

wherein a first quantum well is formed adjacent to the bottom injector layer and the tunnel barrier; and

wherein a second quantum well is formed adjacent to the top injector layer and the tunnel barrier.

Claim 58. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claim 54, 55, 56, or 57, wherein the layers in the interband tunnel diode are grown epitaxially.

Claim 59. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claim 54, 55, 56, or 57, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are a semiconductor or insulator.

Claim 60. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claim 54, 55, 56, or 57, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are comprised of a Group IV alloy.

Application No. 09/934,334 Amendment dated January 6, 2006 Reply to Office Action of September 6, 2005

Claim 61. (Previously Amended)

The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, or 57, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are comprised of, but not limited to, Si, Ge, C, Sn, Si_{1-x}Ge_x, Si_{1-x}C_x, Si₁. _xSn_x, Si_{1-x-y}Ge_xC_y, Si_{1-x-y-z}Ge_xC_ySn_z, Si_{1-x}O_x, Si_{1-x}N_x, A1_{1-x}O_x, or combinations thereof.

Claim 62. (Previously Amended)

The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, or 57, wherein the layers in the interband tunnel diode are grown in a molecular beam epitaxial (MBE) growth system.

Claim 63. (Previously Amended)

The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, or 57, wherein the layers in the interband tunnel diode are grown in a chemical vapor deposition (CVD) growth system.

Claim 64. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, or 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode.

Claim 65 (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, or 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode, using an inert or reducing atmospheres, or moreover a reduction in ambient gas pressure at a temperature in the range of 300 to 1000°C.

Claim 66. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, or 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode, using an

inert or reducing atmosphere, or moreover a reduction in ambient gas pressure at a temperature in the range of 450 to 900°C.

Claim 67. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, or 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of the bottom quantum well layer in the interband tunnel diode.

Claim 68. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, or 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of

the top and bottom quantum well layers, the top and bottom spacer layers, or the tunnel barrier in the interband tunnel diode.

Docket No.: 3531-0103P

Claim 69. (Original)

The method of fabricating an interband tunnel diode as recited in claim 58, wherein the epitaxial growth system occurs over a substrate temperature range between 50°C and 900°C during growth of the layers in the interband tunnel diode.

Claim 70. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of lowering the <u>a</u> substrate temperature before or during growth of the bottom injector layer in the interband tunnel diode.

Claim 71. (Currently Amended)

A method of fabricating an interband tunnel diode comprising the step of lowering the a substrate temperature before or during growth of each of the layers in the interband tunnel diode.

Claim 72. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of elevating the <u>a</u> substrate temperature during or after growth of the bottom injector layer in the interband tunnel diode.

Application No. 09/934,334 Amendment dated January 6, 2006 Reply to Office Action of September 6, 2005

Claim 73. (Currently Amended)

The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of elevating the <u>a</u> substrate temperature during or after growth of the bottom quantum well in the interband tunnel diode.

Claim 74. (Currently Amended)

A method of fabricating an interband tunnel diode by heat treating, during or after growth of <u>each of</u> the layers in the interband tunnel diode.

Claim 75. (Original)

A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode using an inert or reducing atmosphere, or moreover a reduction in ambient gas pressure.

Claim 76. (Original)

A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode at a temperature in the range of 300 to 1000°C.

Claim 77. (Original)

A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode at a temperature in the range of 450 to 900°C.

Application No. 09/934,334 Amendment dated January 6, 2006 Reply to Office Action of September 6, 2005

Claim 78. (Original)

A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode at a temperature in the range of 600 to 800°C.

Claim 79. (Original)

A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode for up to 6 hours.

Claim 80. (Original)

A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode for up to 1 hour.

Claim 81. (Original)

A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode for up to 10 minutes.

Claim 82. (Original)

A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode for up to 2 minutes.

Docket No.: 3531-0103P

Claim 83. (Withdrawn)

A method of fabricating an interband tunnel diode having a p-n junction by growing at least one quantum well epitaxially at a substrate temperature lowered to a predetermined threshold.

Claim 84. (Withdrawn)

A method of fabricating an interband tunnel diode as recited in claim 83 by growing at least one quantum well epitaxially while maintaining a substrate temperature between 0°C and 900°C.

Claim 85. (Withdrawn)

A method of fabricating an interband tunnel diode as recited in claim 83 by growing at least one quantum well epitaxially while maintaining a substrate temperature between 20°C and 500°C.

Claim 86. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claim 71, wherein the layers in the interband tunnel diode are grown epitaxially.

Claim 87. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claim 71 wherein the substrate temperature is lowered at a temperature in the range of 0°C to 900°C.

Claim 88. (Previously Presented)

The method of fabricating an interband tunnel diode as recited in claim 71 wherein the substrate temperature is lowered at a temperature in the range of 0°C to 500°C.

Claim 89. (Previously Presented)

A method of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 6 hours.

Claim 90. (Original)

A method of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 1 hour.

Claim 91. (Previously Presented)

A method of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 10 minutes.

Claim 92. (Previously Presented)

A method of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 2 minutes.